SD11202IQ Power Module

High Input Voltage, 2A Buck Converter with Integrated Inductor - 1

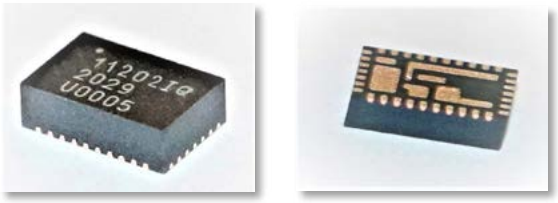
Description

The SD11202IQ Power Module is a high efficiency, synchronous step-down (Buck) DC-DC converter capable of delivering 2A continuous current. The SD11202IQ is assembled in an advanced 6mm x 4mm x 1.85mm 34-pin QFN package, that integrates an inductor, MOSFET switches, small-signal circuits, and compensation.

The SD11202IQ Power Module operates over an input voltage range up to 16V and applies a Constant-on-time (COT) control scheme which provides very fast load transient response and easy loop design. It integrates full protection features, including short-circuit protection, over-current protection, under voltage protection, and thermal shutdown to make the part operate safely.

The SD11202IQ Power Module requires a minimal number of readily available, standard, external components which significantly helps in system design and productivity by offering greatly simplified board design, layout, and manufacturing requirements. In addition, a reduction in the number of components required for the complete power solution helps to enable an overall system cost saving. The SD11202IQ Power Module is RoHS compliant and lead-free manufacturing environment compatible.

Module Form Factor



6x4 QFN Package

Application

- Point of Load Conversion for 7V - 16V input rail
- Space constrained and noise sensitive applications
- High Thermal requirement applications
- Storage (SSD, HDD), Embedded, LV I/O System Power
- FPGAs, ASICs, DSPs, Network processors, Industrial applications
- Security Cameras, Test and Measurement, Portable devices, Medical devices

Features

- Excellent Ripple (<2mV) and Transient Performance
- Up to 2A Continuous Operating Current
- Up to 16V Input Voltage Range
- 1.5% Vfb Initial Accuracy
- 890kHz Switching Frequency
- Optimized Solution Size
- Thermal, Over-Current, Short Circuit, Under-Voltage and Pre-Bias Protections
- 455µA Low Quiescent Current
- RoHS Compliant, MSL Level 3, 260°C Reflow

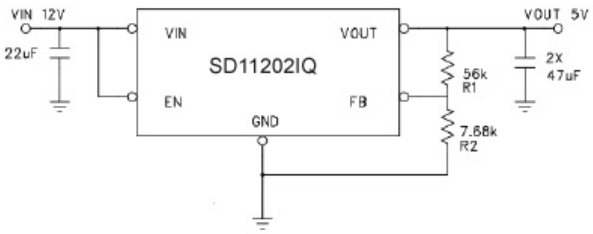


Figure 1: Simplified Applications Circuit

Ordering Information

Part Number	Package Marking	T_A Rating	Package Description
SD11202IQ	11202IQ	-40°C ≤ T_A ≤ 85°C	6mm x 4mm x 1.85mm 34-pin QFN
SD11202IQ-EVB	11202IQ	Customer Evaluation Board	

Pin Functions

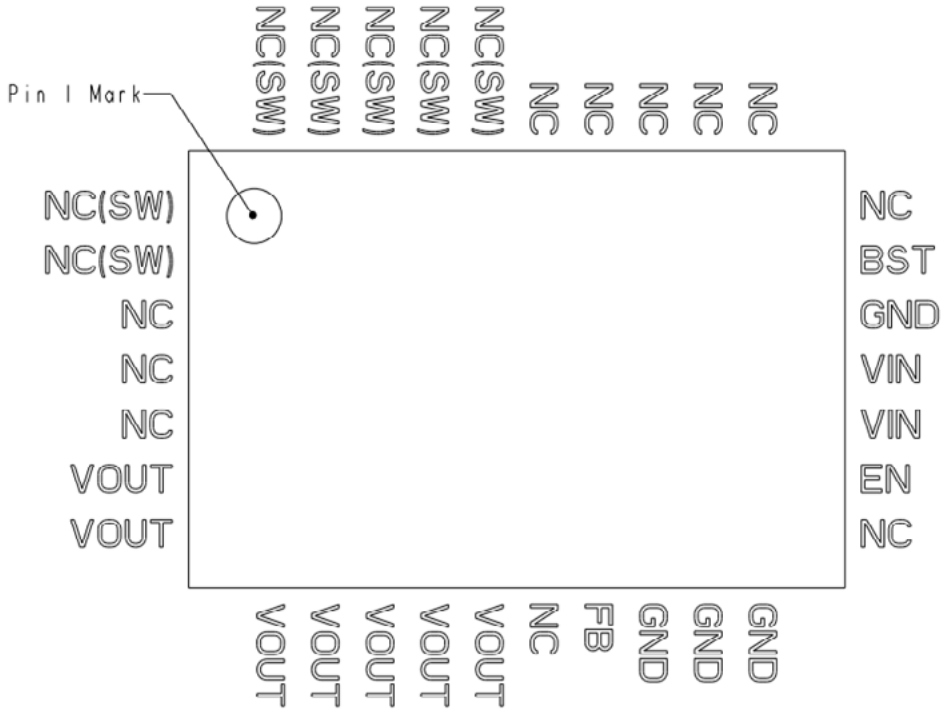


Figure 2: Pin Diagram (Top View)

NOTE A: NC pins are not to be electrically connected to each other or to any external signal, ground or voltage. However, they must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage.

NOTE B: White 'dot' on top left is pin 1 indicator on top of the device package.

Pin Descriptions

PIN	NAME	FUNCTION
1, 2, 30, 31, 32, 33, 34	NC(SW)	No Connect. These pins are internally connected to the common switching node of the internal MOSFETs. They must be soldered to PCB but not be electrically connected to any external signal, ground, or voltage. Failure to follow this guideline may result in device damage.
3, 4, 5,13,18,24,25 26,27,28,29	NC	No Connect. These pins must be soldered to PCB but not electrically connected to each other or to any external signal, voltage, or ground. These pins may be connected internally. Failure to follow this guideline may result in device damage.
6, 7, 8, 9,10,11,12	VOUT	Regulated converter output. Connect to the load and place output filter capacitor(s) between these pins and GND pins. Refer to the Layout Recommendation section.
15,16,17,22	GND	Input/Output power ground. Connect to the ground electrode of the input and output filter capacitors. See VOUT and VIN pin descriptions for more details.
20, 21	VIN	Input power supply. Connect to input power supply. Decouple with input capacitor to GND pin. Refer to the Layout Recommendation section.
19	EN	Enable pin. Applying logic high to the EN pin will enable the device and initiate a soft-start. Applying logic low disables the output and switching stops. EN can be connected to VIN directly or through a resistor.
14	FB	External feedback input pin. Connect resistor between FB and GND, and another resistor between FB to VOUT to set the output voltage. Refer to Output Voltage Setting in page 15 for a description of resistor selection.
23	NC(BST)	Bootstrap pin. This pin is internally connected to a capacitor to SW to form a floating supply across the high-side switch driver. This pin must be soldered to PCB but not be electrically connected to any external signal, ground, or voltage. Failure to follow this guideline may result in device damage.

Absolute Maximum Ratings

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond the recommended operating conditions is not implied. Stress beyond the absolute maximum ratings may impair device life. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Absolute Maximum Pin Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Voltage	VIN	-0.3	18.0	V
Device Enable	EN	-0.3	V_{IN}+0.3	V
Feedback	FB	-0.3	5.5	V
Switch Node	NC(SW) Voltage DC		18.0	V
BOOST	NC(BST)	-0.3	18.0	V

Absolute Maximum Thermal Ratings

PARAMETER	CONDITION	MIN	MAX	UNITS
Maximum Operating Junction Temperature			+150	°C
Storage Temperature Range		-65	+150	°C
Reflow Peak Body Temperature	(10 Sec) MSL3 JEDEC J-STD-020A		+260	°C

Absolute Minimum ESD Ratings

PARAMETER	CONDITION	MIN	MAX	UNITS
HBM (Human Body Model)		±2000		V
CDM (Charged Device Model)		±500		V

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Voltage Range	V_{IN}	7	16	V
Output Voltage Range	V_{OUT}	0.6	5.0	V
Output Current Range	I_{OUT}		2	A
Operating Junction Temperature	T_J	-40	+125	°C

Thermal Characteristics

PARAMETER	SYMBOL	TYPICAL	UNITS
Thermal Shutdown	T_{SD}	150	°C
Thermal Shutdown Hysteresis	T_{SDHYS}	20	°C
Thermal Resistance: Junction to Ambient (0 LFM) (1)	θ_{JA}	19	°C/W
Thermal Resistance: Junction to Case (0 LFM)	θ_{JC}	1	°C/W

(1) Based on 2oz. external copper layers and proper thermal design in line with EIJ/JEDEC JESD51-7 standard for high thermal conductivity boards.

Electrical Characteristics

NOTE: V_{IN} = 12V, Minimum and Maximum values are over operating ambient temperature, vin, and load range unless otherwise noted. Typical values are at $T_A = T_J = 25°C$.

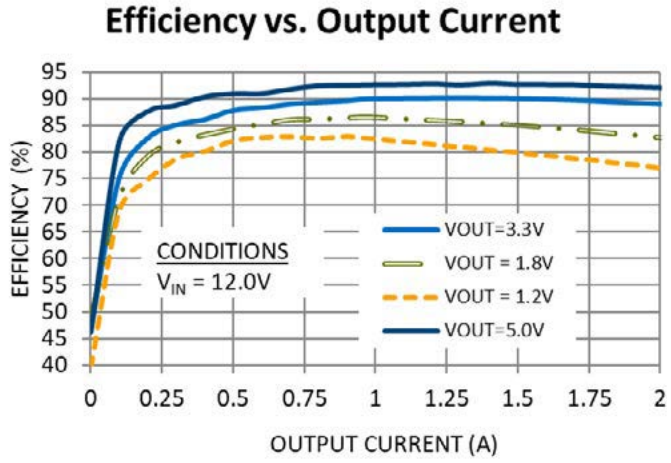
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Input Voltage (1)	V_{IN}		7		16	V
Under Voltage Lock-Out – V_{IN} Rising	V_{UVLOR}	Voltage above which UVLO is not asserted	4.1	4.13	4.22	V
Under Voltage Lock-Out – V_{IN} Falling	V_{UVLOF}	Voltage below which UVLO is asserted	3.8	3.93	4.05	V
Under Voltage Lock-Out Hysteresis	$V_{UVLOHYS}$			200		mV
Shut-Down Supply Current	I_S	EN = 0V			10	µA
No Load Quiescent Current	I_{VINQ}	V_{OUT} = 1.2V	210	455	895	µA
Feedback Pin Voltage (2)	V_{FB}	V_{OUT} = 0.6V, I_{LOAD} = 0, T_A =25°C	0.596	0.605	0.614	V
Feedback Pin Voltage (Line, Load, Temp.)	V_{FB}	$7V \leqslant V_{IN} \leqslant 16V$ $0A \leq I_{LOAD} \leq 2A$; $-40°C \leq T_A \leq 85°C$	0.593	0.605	0.617	V
Feedback pin Input Leakage Current (3)	I_{FB}	VFB pin input leakage current		18	60	nA
V_{OUT} Rise Time (3)	t_{RISE}			0.8	1.5	ms
Continuous Output Current	I_{OUT}		0		2	A
Valley Current Limit Trip Level	I_{OCP}	V_{IN} = 12V, V_{OUT} = 1.2V	4.2	4.5		A
Current Limit Retry Time (3)	T_{CL_TRY}			2.5		ms
Disable Threshold	$V_{DISABLE}$	EN pin logic going low		1.05		V
Enable Threshold	V_{EN}	EN pin logic going high	1.1	1.2	1.4	V
EN Hysteresis	EN_{HYS}			150		mV
EN Pin Input Current	I_{EN}	EN = 2.0V		1.5	2	µA
Switching Frequency	F_{SW}	Free running frequency of oscillator		890		kHz

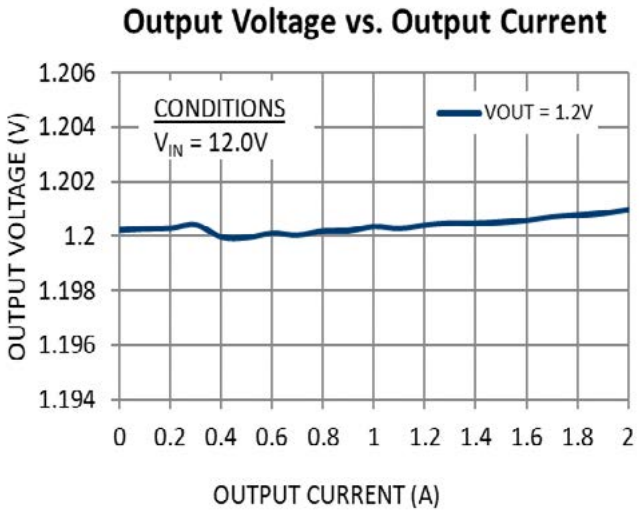
(1) Minimum Vin voltage must be at least 1.3V higher than Vout.

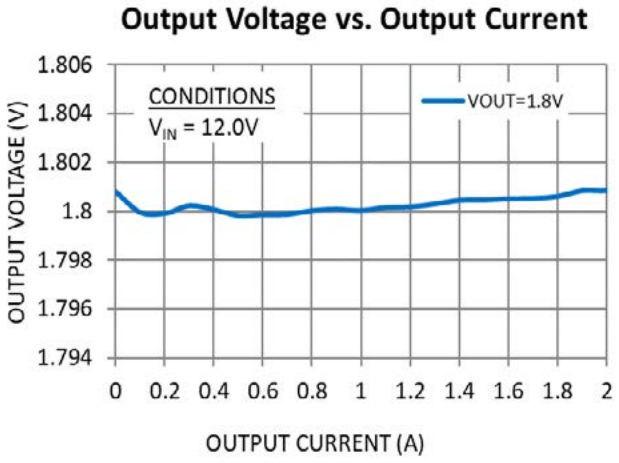
(2) The FB pin is a sensitive node. Do not touch FB while the device is in regulation.

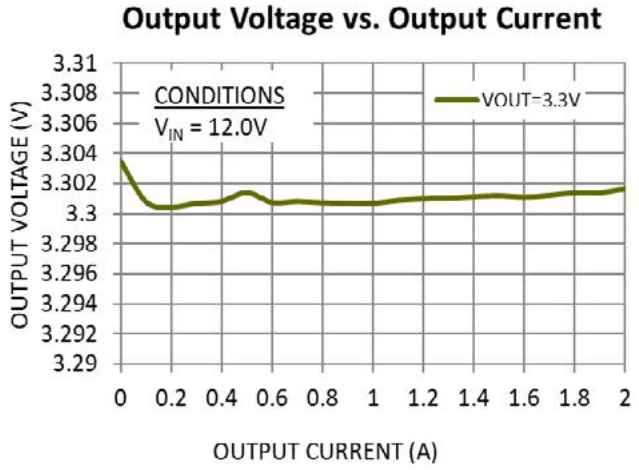
(3) Parameter not production tested but is guaranteed by design.

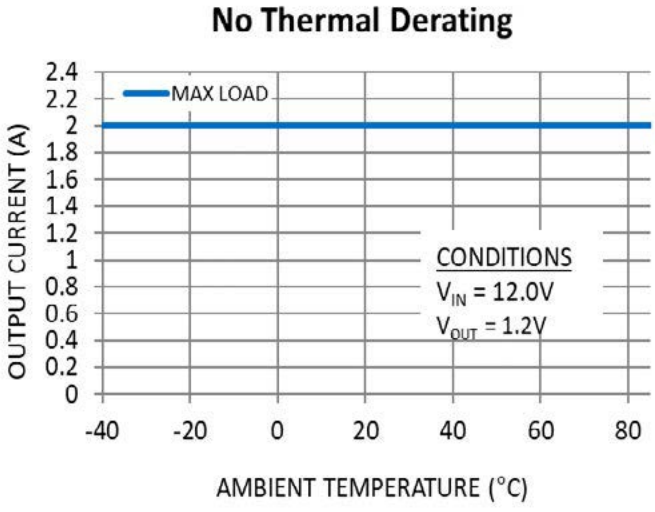
Typical Performance Curves

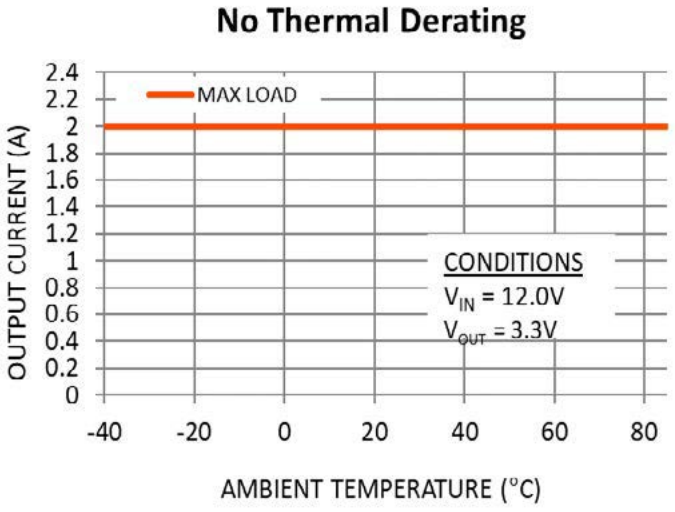




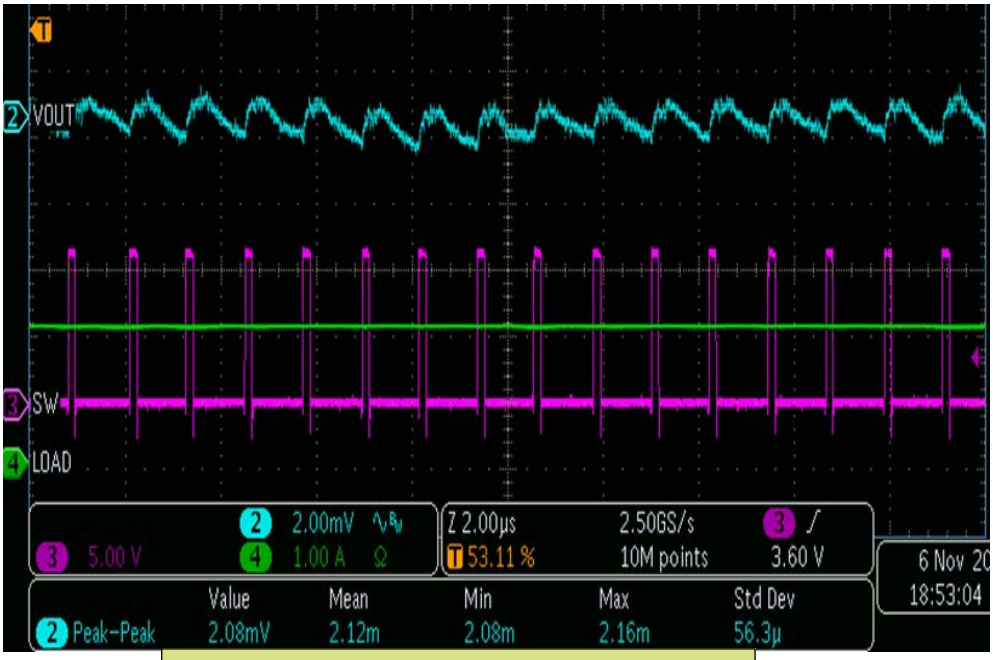




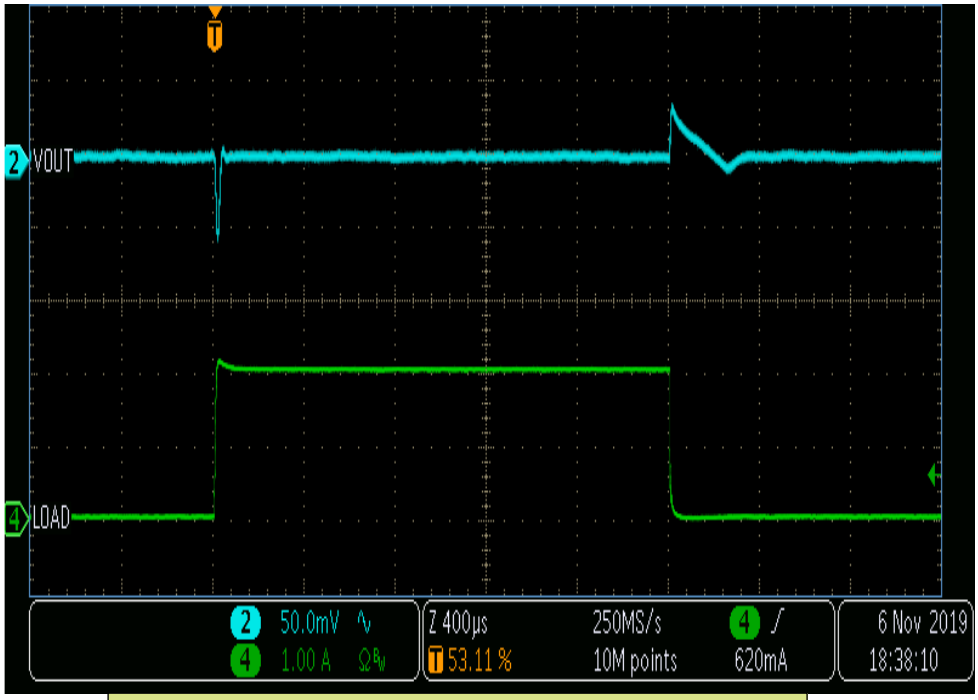




Typical Performance Characteristics

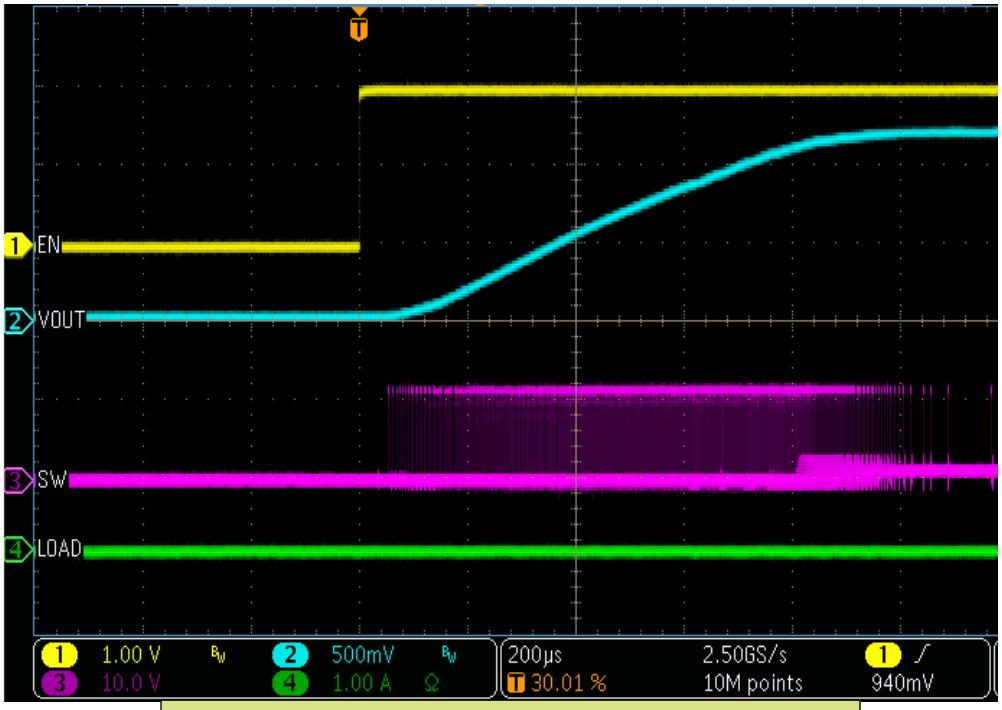


OUTPUT Ripple, 12V Vin, 1.2V Vout, 2A DC



Load Transient Response, 12V Vin, 1.2V Vout, 2A DC

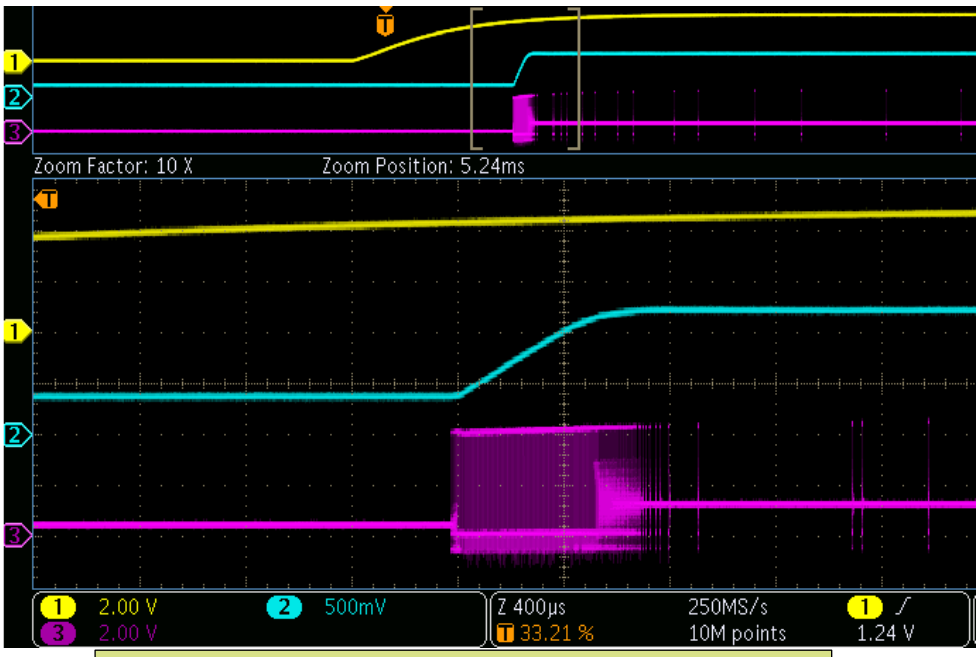
Typical Performance Characteristics (Continued)



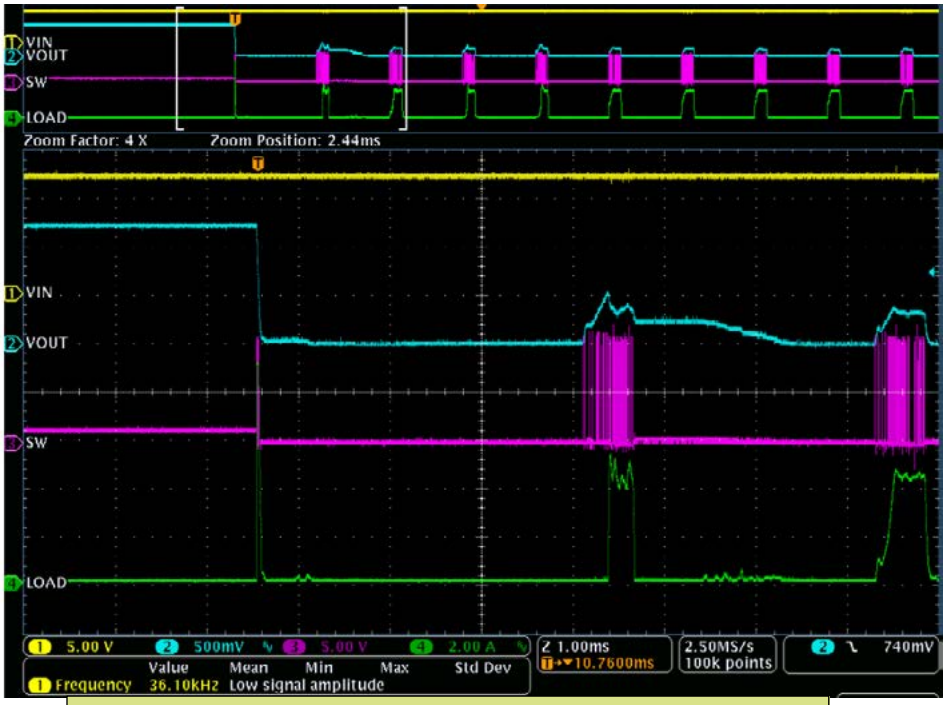
Startup, 12V Vin, 1.2V Vout, No LOAD

Shutdown, 12V Vin, 1.2V Vout, No LOAD

Typical Performance Characteristics (Continued)

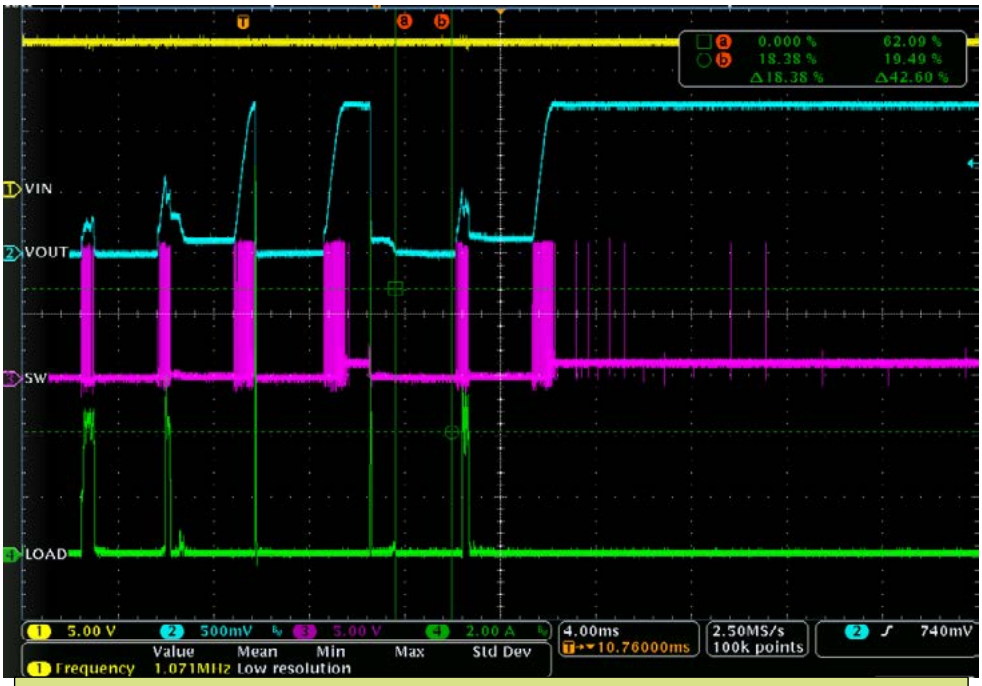


Pre-bias start up (~400mV), 12V Vin, 1.2V Vout Vout (Ch2), SW (Ch3), Vin(Ch1)

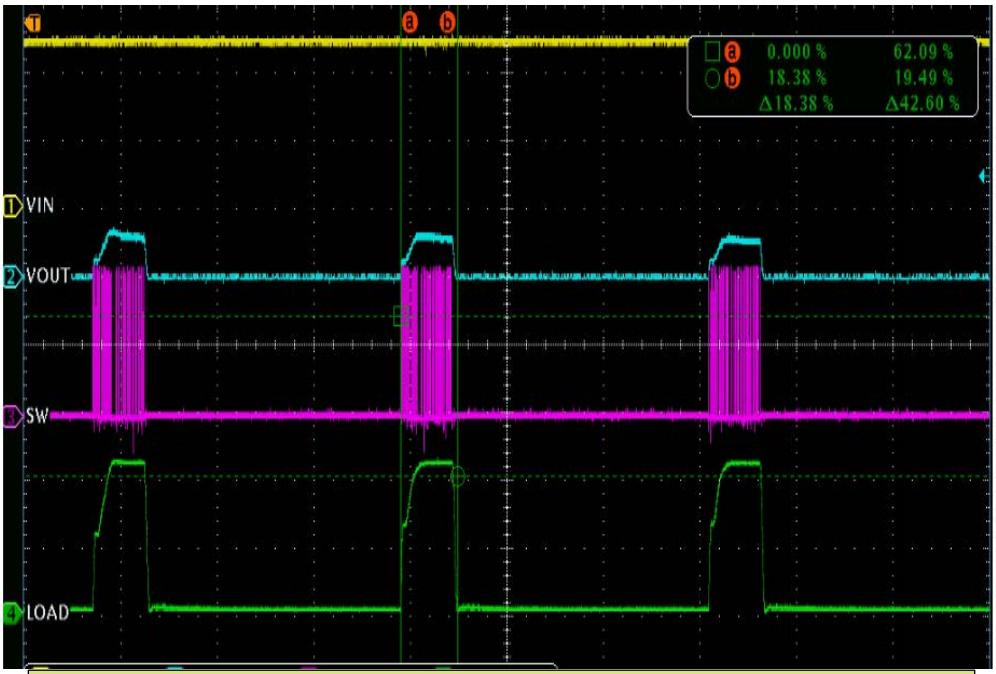


Short Circuit RESPONSE, 12V Vin, 1.2V Vout

Typical Performance Characteristics (Continued)



Short Circuit RECOVERY, 12V Vin, 1.2V Vout



Short Circuit Hiccup Mode, 12V Vin, 1.2V Vout

Functional Block Diagram

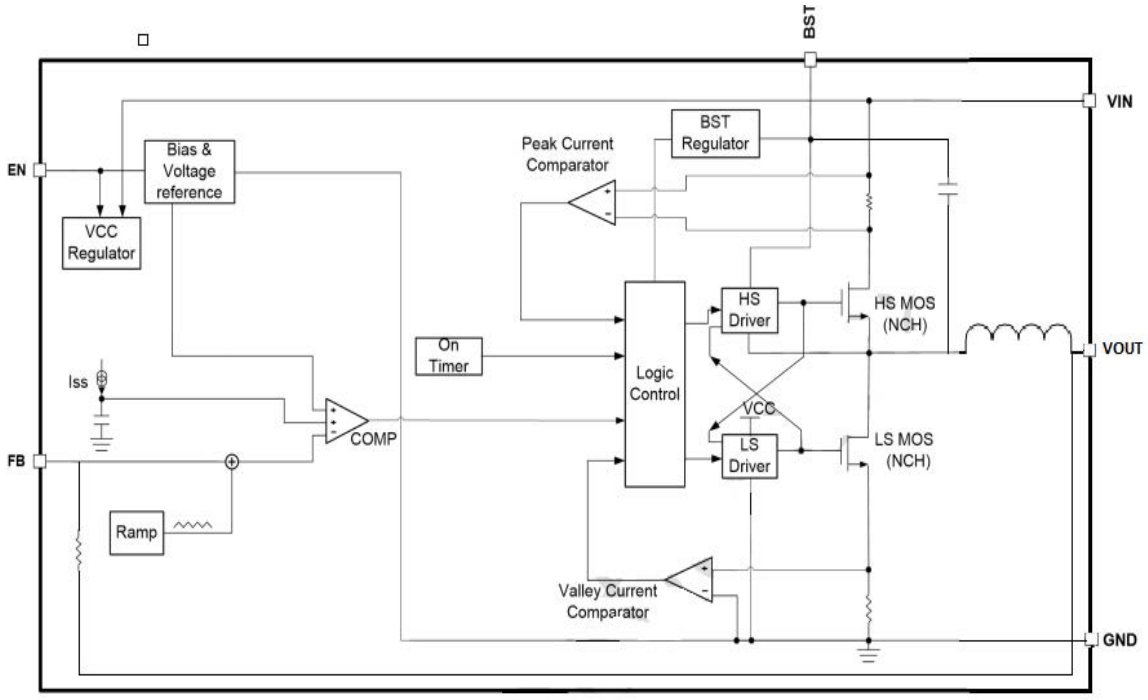


Figure 3: Functional Block Diagram

Functional Description

The SD11202IQ is a fully integrated, synchronous, rectified, step-down, switch-mode converter. Constant-on-time (COT) control is employed to provide fast transient response and to simplify loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned on when the FB voltage (VFB) drops below the reference voltage (VREF). The HS-FET is turned on for a fixed interval determined by the one-shot on-timer. The on-timer is determined by both the output voltage and input voltage to make the switching frequency fairly constant over the input voltage range. After the on period elapses, the HS-FET is turned off until the next period begins. By repeating this operation, the converter regulates the output voltage. Continuous conduction mode (CCM) occurs when the output current is high and the inductor current is always above zero amps. The low side MOSFET is turned on when the high side MOSFET is in its off state to minimize conduction loss. To prevent a shoot-through (a short between the input and GND if both the HS-FET and LS-FET are turned on at the same time), a dead time is generated internally between the HS-MOSFET off and LS-MOSFET on, or LS-MOSFET off and HS-MOSFET on.

When the SD11202IQ works in PFM mode during light-load operation, the SD11202IQ reduces the switching frequency automatically to maintain high efficiency, and the inductor current drops almost to zero. When the inductor current reaches zero, the low-side driver enters tri-state (high-Z). The output capacitors discharge slowly to GND through FB divider resistors. When VFB drops below the reference voltage, the HS-FET is turned on. This operation improves device efficiency greatly when the output current is low. During Light-load operation, the HS-FET does not turn on as frequently as it does in heavy-load conditions.

The frequency at which the HS-FET turns on is a function of the output current. As the output current increases, the time period that the current modulator regulates becomes shorter, and the HS-FET turns on more frequently. The switching frequency increases in turn. The output current reaches critical levels when the current modulator time is zero, and can be determined with Equation (1):

$$Iout = \frac{(Vin - Vout)\ x\ Vout}{2\ x\ L\ x\ Fsw\ x\ Vin}$$

The SD11202IQ reverts to PWM mode once the output current exceeds the critical level. Afterward, the switching frequency remains fairly constant over the output current range.

Under-Voltage Lockout (UVLO)

Under-voltage lock out protection (UVLO) monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut down. This protection is non-latching.

Enable (EN) Control

Enable (EN) is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. An internal 770 kΩ resistor from EN to GND allows EN to be floated to shut down the chip. EN is clamped internally using a 3V series Zener diode. EN can be connected to VIN directly to save one pull up resistor.

Over-Current Protection (OCP) and Short Circuit Protection (SCP)

The SD11202IQ has valley current-limit control. During LS-FET on, the inductor current is monitored. When the sensed inductor current reaches the valley current limit, the LS-MOSFET limit comparator turns over. The device enters over current protection (OCP) mode and the HS-FET waits until the valley current limit disappears before turning on again. The output voltage drops until VFB is below the under voltage (UV) threshold (typically 44% below the reference). Once UV is triggered, the SD11202IQ enters hiccup mode to restart the part periodically. During OCP, the device attempts to recover from the over-current fault with hiccup mode. In hiccup mode, the chip disables the output power stage, discharges the soft start, and attempts to soft start again automatically. If the over-current condition still holds after the soft start ends, the device repeats this operation cycle until the over-current condition is removed and the output rises back to regulation levels. OCP is a non-latch protection.

Soft Start and Pre-Biased Soft Start

Soft start (SS) prevents the converter output voltage from overshooting and input inrush current during start-up. The SD11202IQ has an internal 0.8ms soft-start. When the EN pin becomes high, the internal soft-start function begins ramping up the reference voltage to the PWM comparator. If the output capacitor is pre-biased at startup, the devices initiate switching and start ramping up only after the internal reference voltage becomes greater than the feedback voltage VFB. This scheme ensures that the converters ramp up smoothly into regulation point.

Thermal-Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. The device monitors the temperature of itself. If the temperature exceeds the threshold value (typically 150°C), the device is shut off. This is a non-latch protection.

Application Information

Output Voltage Setting

The SD11202IQ output voltage is programmed by setting two resistors, one resistor between FB and VOUT (R_1) and one resistor between FB and GND (R2). Figure 5 shows the resistor configuration. It is recommended to use 56kΩ for R1 and adjust R2 to set the output voltage.

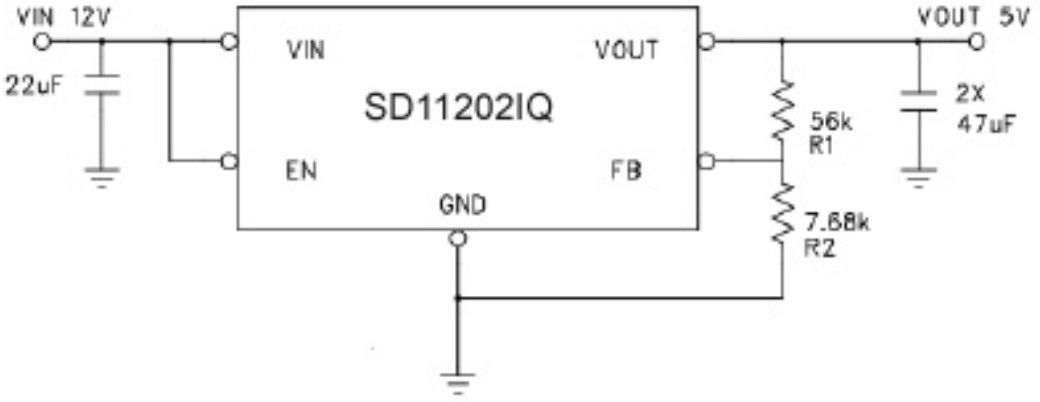


Figure 4: Typical Applications Circuit

Depending on input and output voltage, the recommended external passive component values are shown in Table 1.

V_{IN}	V_{OUT}	R_1	R_2	C_{OUT}
12V	0.6V	56kΩ	OPEN	2 x 47µF
	1.2V	56kΩ	56kΩ	
	1.8V	56kΩ	28.4kΩ	
	3.3V	56kΩ	12.6kΩ	
	5.0V	56kΩ	7.68kΩ	

Table 1: Common external passive component settings

Setting other Output Voltages

To choose output voltage settings other than those stated in table 1, assume R1= 56kΩ, choose resistor between FB and GND (R_2), per the formula below:

$$R2 = \frac{33.88}{Vout - 0.605}$$

Input Capacitor Selection

The input of synchronous buck regulators can be very noisy and should be decoupled properly in order to ensure stable operation. In addition, input parasitic line inductance can attribute to higher input voltage ripple. It is recommended to have a minimum of 22µF input capacitance. For improved transient response, use a 100uF input capacitor.

As the distance of the input power source to the input of the SD11202IQ is increased, it is recommended to increase input capacitance in order to mitigate the line inductance from the source. Low-ESR ceramic capacitors should be used. The dielectric must be X5R or X7R rated and the size must be at least 0805 (EIA) due to derating. Y5V or equivalent dielectric formulations must not be used as these lose too much capacitance with frequency, temperature and bias voltage. In some applications, lower value capacitors are needed in parallel with the larger capacitors in order to provide high frequency decoupling. Larger electrolytic or tantalum bulk capacitors may be used in conjunction to increase total input capacitance but should not be used solely as a replacement for the ceramic capacitors.

Output Capacitor Selection

The output ripple of a synchronous buck converter can be attributed to its inductance, switching frequency and output decoupling. It is recommended to have a minimum of 2 x 47µF output capacitors. For improved transient response, use two 47uF in parallel with one 100uF capacitor.

Low ESR ceramic capacitors should be used. The dielectric must be X5R or X7R rated and the size must be at least 0805 (EIA) due to derating. Y5V or equivalent dielectric formulations must not be used as these lose too much capacitance with frequency, temperature and bias voltage.

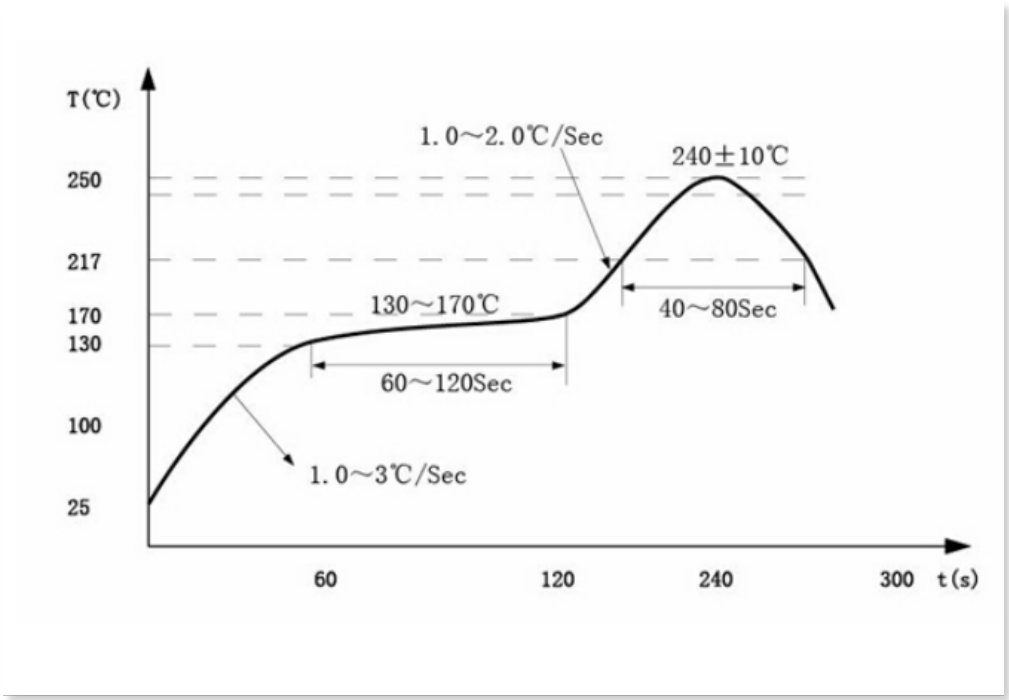


Figure 5: IR Reflow Profile for the 6x4 QFN Package

Layout Recommendations

Recommendation 1: Input and output filter capacitors should be placed on the same side of the PCB, and as close to the SD11202IQ package as possible. They should be connected to the device with very short and wide traces. Do not use thermal reliefs or spokes when connecting the capacitor pads to the respective nodes. The Voltage and GND traces between the capacitors and the SD11202IQ should be as close to each other as possible so that the gap between the two nodes is minimized, even under the capacitors.

Recommendation 2: Half of the PGND pins are dedicated to the input circuit and the other half to the output circuit. Incorporting a slit separating the input and output GND circuits helps minimize noise coupling between the converter input and output switching loops.

Recommendation 3: The system ground plane should be on the 2nd layer (below the surface layer). This ground plane should be continuous and un-interrupted.

Recommendation 4: The large thermal pad underneath the device must be connected to the system ground plane through as many vias as possible. The drill diameter of the vias should be 0.33mm, and the vias must have at least 1-oz. copper plating on the inside wall, making the finished hole size around 0.2mm to 0.26mm. Do not use thermal reliefs or spokes to connect the vias to the ground plane. This connection provides the path for heat dissipation from the converter.

Recommendation 5: Multiple small vias (the same size as the thermal vias discussed in recommendation 4 should be used to connect ground terminal of the input capacitor and output capacitors to the system ground plane. Put the vias under the capacitors along the edge of the GND copper closest to the Voltage copper. These vias connect the input/output filter capacitors to the GND plane, and help reduce parasitic inductance in the input and output current loops. If the vias cannot be placed under C_{IN} and C_{OUT}, then put them just outside the capacitors along the GND slit separating the two components. Do not use thermal reliefs or spokes to connect these vias to the ground plane.

Recommendation 6: The V_{OUT} sense point should be connected at the last output filter capacitor furthest from the VOUT pins. Keep the sense trace as short as possible in order to avoid noise coupling into the control loop.

Recommendation 7: As with any switch-mode DC-DC converter, try not to run sensitive signal or control lines underneath the converter package on other layers.

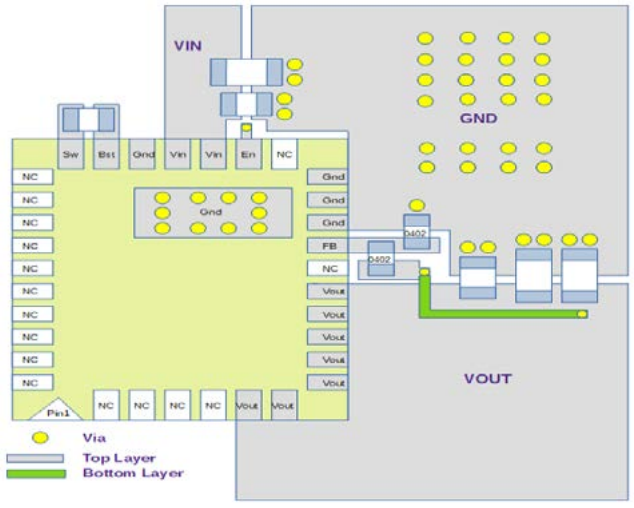
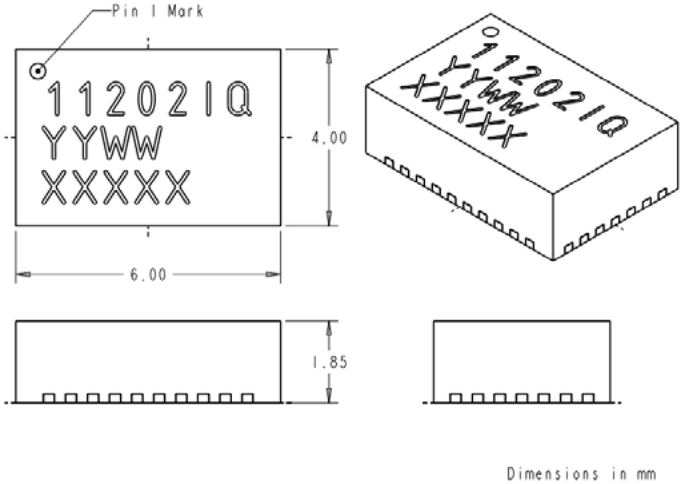


Figure 6: Recommended PCB Layout

Package drawings



Design considerations for Lead-frame based modules

Exposed Metal on Bottom of Package

Only the thermal pad and the perimeter pads are to be mechanically or electrically connected to the board. The PCB top layer under the SD11202IQ should be clear of any metal (copper pours, traces, or vias) except for the thermal pad. The "shaded-out" area in Figure 9 represents the area that should be clear of any metal on the top layer of the PCB. Any layer 1 metal under the shaded-out area runs the risk of undesirable shorted connections even if it is covered by solder mask.

The solder stencil aperture should be smaller than the PCB ground pad. This will prevent excess solder from causing bridging between adjacent pins or other exposed metal under the package.

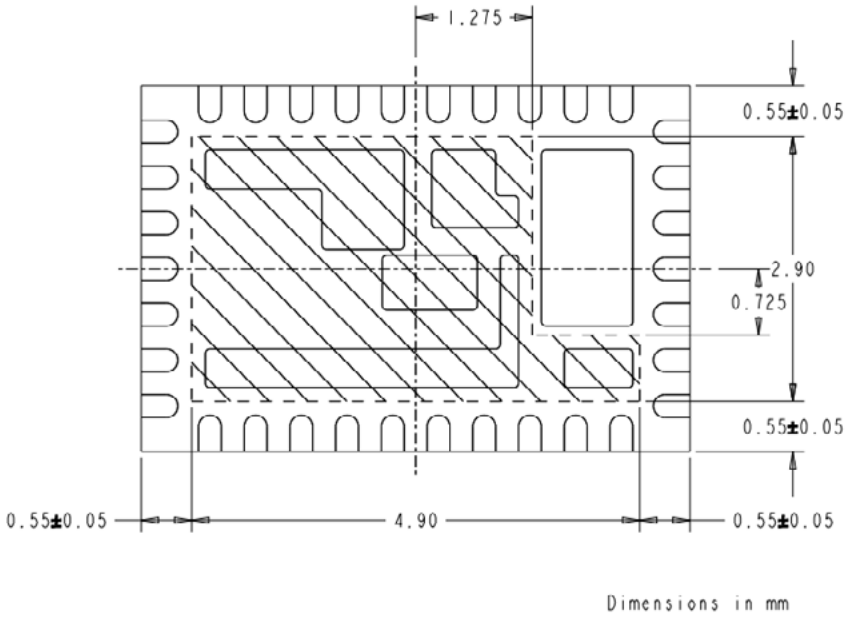


Figure 7: Lead-Frame exposed metal (Bottom View)

Shaded area highlights exposed metal that is not to be mechanically or electrically connected to the PCB.

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