

# PRODUCT CATALOG

## N-CHANNEL ENHANCEMENT MOS FET

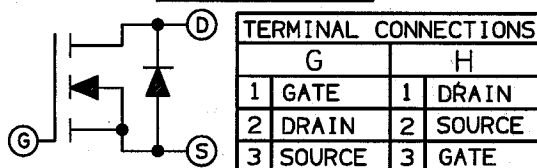
1000V, 9A, 1.4 Ω

SDF9N100 GAF

### FEATURES

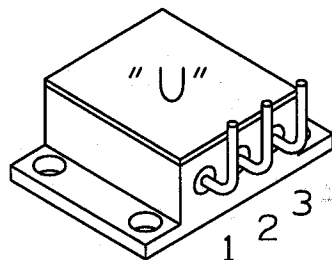
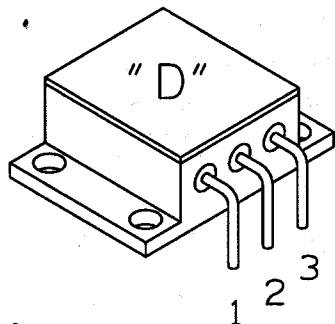
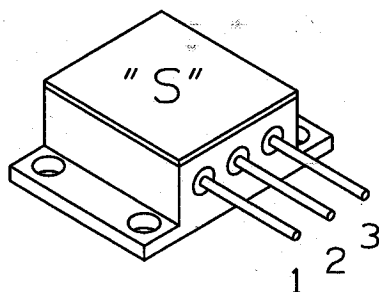
- RUGGED PACKAGE
- HI-REL CONSTRUCTION
- CERAMIC EYELETS
- LEAD BENDING OPTIONS
- COPPER CORED 52 ALLOY PINS
- LOW IR LOSSES
- LOW THERMAL RESISTANCE
- OPTIONAL MIL-S-19500 SCREENING

### SCHEMATIC



STANDARD BEND CONFIGURATIONS

GAF



(CUSTOM BEND OPTIONS AVAILABLE)

### ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL		UNITS
Drain-source Volt.(1)	V <sub>DSS</sub>	1000	Vdc
Drain-Gate Voltage (R <sub>GS</sub> =1.0M $\Omega$ ) (1)	V <sub>DGR</sub>	1000	Vdc
Gate-Source Voltage Continuous	V <sub>GS</sub>	$\pm 20$	Vdc
Drain Current Continuous (T <sub>c</sub> = 25°C)	I <sub>D</sub>	9	Adc
Drain Current Pulsed(3)	I <sub>DM</sub>	36	A
Total Power Dissipation	PD	300	W
Power Dissipation Derating > 25°C		2.4	W/°C
Operating & Storage Temp.	T <sub>J</sub> /T <sub>sig</sub>	-55 TO +150	°C
Thermal Resistance	R <sub>thJc</sub>	0.42	°C/W
Max.Lead temperature	TL	300	°C

### ELECTRICAL CHARACTERISTICS T<sub>c</sub> = 25°C (UNLESS OTHER-WISE SPECIFIED)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Drain-source Breakdown Volt.	V <sub>(BR)DSS</sub>	V <sub>GS</sub> =0V I <sub>D</sub> =250 $\mu$ A	1000	-	-	V
Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>D</sub> =V <sub>GS</sub> I <sub>D</sub> =250 $\mu$ A	2.0	-	4.5	V
Gate Source Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = $\pm 20$ V	-	-	100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>D</sub> =MAX.RATING V <sub>GS</sub> =0 V <sub>D</sub> =0.8 MAX.RATING V <sub>GS</sub> =0 T <sub>J</sub> =125°C	-	-	250	$\mu$ A
Static Drain-Source On-State Resistance(1)	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10 V I <sub>D</sub> =4.5A	-	-	1.4	$\Omega$
Forward Trans-Conductance (2)	g <sub>f</sub> s	V <sub>D</sub> $\geq$ 50 V I <sub>D</sub> =4.5A	6.0	-	-	S(U)
Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> =0V V <sub>D</sub> =25 V	-	4500	-	pF
Output Capacitance	C <sub>OSS</sub>	f=1.0 MHz	-	550	-	pF
Reverse Transfer Capacitance	C <sub>RSS</sub>		-	160	-	pF
Turn-On Delay	t <sub>d(on)</sub>	V <sub>D</sub> =500V Z <sub>o</sub> =50 $\Omega$ I <sub>D</sub> =4.5A	-	-	100	ns
Rise Time	t <sub>r</sub>	(MOSFET switching times are essentially independent of operating temp.)	-	-	110	ns
Turn-Off Delay	t <sub>d(off)</sub>		-	-	220	ns
Fall Time	t <sub>f</sub>		-	-	105	ns
Total Gate Charge (Gate-Source Plus Gate-Drain)	Q <sub>g</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =9A	-	145	-	nC
Gate-Source Charge	Q <sub>gs</sub>	V <sub>D</sub> =0.8 MAX.RATING (Gate charge is essentially independent of the operating temperature)	-	55	-	nC
Gate-Drain ("Miller") Charge	Q <sub>gd</sub>		-	90	-	nC

### SOURCE-DRAIN DIODE RATINGS & CHARACT. T<sub>c</sub> = 25°C (UNLESS OTHER-WISE SPECIFIED)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Continuous Source Current (Body Diode)	I <sub>S</sub>	Modified MOSFET symbol showing the integral reverse P-N junction rectifier (See schematic)	-	-	9	A
Pulse Source Current (Body Diode) (1)	I <sub>SM</sub>		-	-	36	A
Diode Forward Voltage (2)	V <sub>SD</sub>	I <sub>F</sub> =9A V <sub>GS</sub> =0V T <sub>c</sub> =+25°C	-	-	1.5	V
Reverse Recovery Time	t <sub>rr</sub>	T <sub>c</sub> =+25°C	-	600	-	ns
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> =9A di/dt=100A/ $\mu$ S	-	8.5	-	$\mu$ C

(1) T<sub>J</sub> = 25°C to 150°C.

(2) Pulse test: Pulse Width < 300 $\mu$ S, Duty Cycle < 2%.

(3) Repetitive Rating: Pulse Width limited By Max. Junction Temperature.