N-CHANNEL ENHANCEMENT MOS FET

1000V, 4.4A, 4.0Ω

SDF4NA100 JAA
SDF4NA100 JAB

FEATURES

- RUGGED PACKAGE
- HI-REL CONSTRUCTION
- CERAMIC EYELETS
- LEAD BENDING OPTIONS
- COPPER CORED 52 ALLOY PINS
- LOW IR LOSSES
- LOW THERMAL RESISTANCE
- OPTIONAL MIL-S-19500 SCREENING (TX-S)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL		UNITS
Drain-Source Volt.(1)	VDSS	1000	Vdc
Drain-Gate Voltage (R_{GS}=1.0Mω) (1)	VDGR	1000	Vdc
Gate-Source Voltage Continuous	VGS	±30	Vdc
Drain Current Continuous (T_C = 25°C)	ID	4.4	Adc
Drain Current Pulsed(3)	IDM	17.6	A
Total Power Dissipation	PD	150	W
Power Dissipation Derating > 25°C		1.2	W/°C
Operating & Storage Temp.	TJ/Tstg	-55 TO +150	°C
Thermal Resistance	RthJc	0.8	°C/W
Max.Lead temperature	TL	300	°C

ELECTRICAL CHARACTERISTICS T_C = 25°C (UNLESS OTHERWISE SPECIFIED)

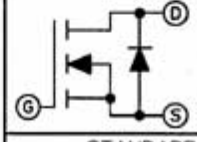
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Drain-source Breakdown Volt.	V(BR)DSS	VGS=0V ID=250 µA	1000	-	-	V
Gate Threshold Voltage	VGS(TH)	VDS=VGS ID=1 MA	2.0	-	4.0	V
Gate Source Leakage	IGSS	VGS=±30 V	-	-	100	nA
Zero Gate Voltage Drain Current	IDSS	VDS=MAX.RATING VGS=0	-	-	250	µA
		VDS=0.8 MAX.RATING VGS=0 TJ=125°C	-	-	1000	µA
Static Drain-Source On-State Resistance(1)	RDS(ON)	VGS=10 V ID=2.2A	-	-	4.0	Ω
Input Capacitance	CISS	VGS=0V VDS=25 V f=1.0 MHz	-	805	-	pF
Output Capacitance	COSS		-	115	-	pF
Reverse Transfer Capacitance	CRSS		-	37	-	pF
Turn-On Delay	td(on)	VDD=500V RG=1.8Ω ID=4.4A VGS=15V (MOSFET switching times are essentially independent of operating temp.)	-	-	23	ns
Rise Time	tr		-	-	20	ns
Turn-Off Delay	td(off)		-	-	50	ns
Fall Time	tf		-	-	27	ns
Total Gate Charge (Gate-Source Plus Gate-Drain)	Qg	VGS=10V, ID=4.4A VDS=0.5 MAX.RATING (Gate charge is essentially independent of the operating temperature)	-	-	55	nC
Gate-Source Charge	Qgs		-	-	6.5	nC
Gate-Drain ("Miller") Charge	Qgd		-	-	27	nC

SOURCE-DRAIN DIODE RATINGS & CHARACT. T_C = 25°C (UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Continuous Source Current (Body Diode)	IS	Modified MOSFET symbol showing the integral reverse P-N junction rectifier (See schematic)	-	-	4.4	A
Pulse Source Current (Body Diode) (1)	ISM		-	-	17.6	A
Diode Forward Voltage (2)	VSD	IF=4.4A VGS=0V TC=+25°C	-	-	1.3	V
Reverse Recovery Time	trr	TC=+25° C IF=4.4A di/dt=100A/µS	-	-	580	ns
Reverse Recovery Charge	Qrr		-	1.65	-	µC

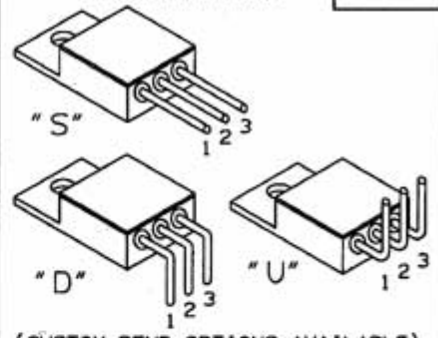
(1) TJ = 25°C to 150°C.
(2) Pulse test: Pulse Width <300µS, Duty Cycle <2%.
(3) Repetitive Rating: Pulse Width limited By Max.junction Temperature.

SCHEMATIC



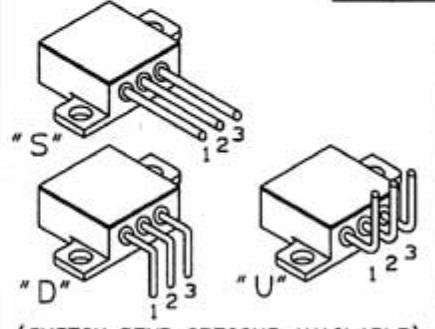
TERMINAL CONNECTIONS			
G		H	
1	GATE	1	DRAIN
2	DRAIN	2	SOURCE
3	SOURCE	3	GATE

STANDARD BEND CONFIGURATIONS — JAA



(CUSTOM BEND OPTIONS AVAILABLE)

STANDARD BEND CONFIGURATIONS — JAB



(CUSTOM BEND OPTIONS AVAILABLE)