

## N-CHANNEL ENHANCEMENT MOS FET

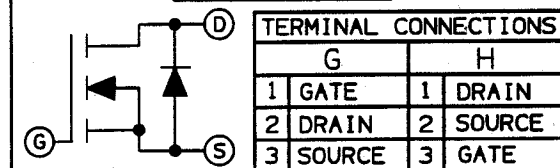
1000V, 4.0A, 3.5Ω

SDF4N100 JAA  
SDF4N100 JAB

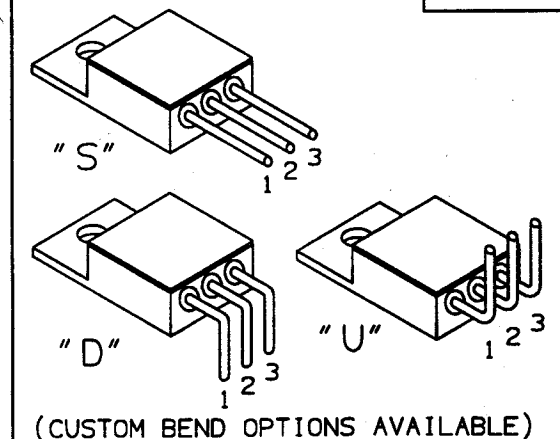
### FEATURES

- RUGGED PACKAGE
- HI-REL CONSTRUCTION
- CERAMIC EYELETS
- LEAD BENDING OPTIONS
- COPPER CORED 52 ALLOY PINS
- LOW IR LOSSES
- LOW THERMAL RESISTANCE
- OPTIONAL MIL-S-19500 SCREENING

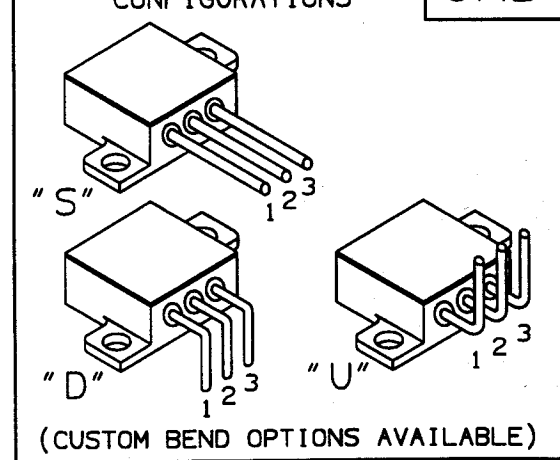
### SCHEMATIC



### STANDARD BEND CONFIGURATIONS



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### ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL		UNITS
Drain-source Volt.(1)	V <sub>DSS</sub>	1000	V <sub>dc</sub>
Drain-Gate Voltage (R <sub>GS</sub> =1.0MΩ) (1)	V <sub>DGR</sub>	1000	V <sub>dc</sub>
Gate-Source Voltage Continuous	V <sub>GS</sub>	±20	V <sub>dc</sub>
Drain Current Continuous (T <sub>c</sub> = 25°C)	I <sub>D</sub>	4.0	A <sub>dc</sub>
Drain Current Pulsed(3)	I <sub>DM</sub>	16	A
Total Power Dissipation	P <sub>D</sub>	100	W
Power Dissipation Derating > 25°C		0.83	W/°C
Operating & Storage Temp.	T <sub>J</sub> /T <sub>stg</sub>	-55 TO +150	°C
Thermal Resistance	R <sub>thJc</sub>	1.2	°C/W
Max.Lead temperature	TL	300	°C

### ELECTRICAL CHARACTERISTICS T<sub>c</sub> = 25°C (UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Drain-source Breakdown Volt.	V <sub>(BR)</sub> DSS	V <sub>GS</sub> =0V I <sub>D</sub> =250 μA	1000	-	-	V
Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>D</sub> =V <sub>GS</sub> I <sub>D</sub> =250 μA	2.0	-	4.5	V
Gate Source Leakage	I <sub>GSS</sub>	V <sub>GS</sub> =±20 V	-	-	100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>D</sub> =MAX.RATING V <sub>GS</sub> =0 V <sub>D</sub> =0.8 MAX.RATING T <sub>J</sub> =125°C	-	-	250 1000	μA
Static Drain-Source On-State Resistance(1)	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10 V I <sub>D</sub> =2.0A	-	-	3.5	Ω
Forward Trans-Conductance (2)	g <sub>fs</sub>	V <sub>D</sub> ≥ 15 V I <sub>D</sub> =2.0A	3.5	-	-	S(U)
Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> =0V V <sub>D</sub> =25 V f=1.0 MHz	-	1500	-	pF
Output Capacitance	C <sub>OSS</sub>		-	100	-	pF
Reverse Transfer Capacitance	C <sub>RSS</sub>		-	30	-	pF
Turn-On Delay	t <sub>d(on)</sub>	V <sub>D</sub> =500V Z <sub>o</sub> =10 Ω I <sub>D</sub> =2.0A (MOSFET switching times are essentially independent of operating temp.)	-	-	40	ns
Rise Time	t <sub>r</sub>		-	-	60	ns
Turn-Off Delay	t <sub>d(off)</sub>		-	-	170	ns
Fall Time	t <sub>f</sub>		-	-	60	ns
Total Gate Charge (Gate-Source Plus Gate-Drain)	Q <sub>g</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =4.0A V <sub>D</sub> =0.4 MAX.RATING (Gate charge is essentially independent of the operating temperature)	-	-	120	nC
Gate-Source Charge	Q <sub>gs</sub>		-	-	15	nC
Gate-Drain ("Miller") Charge	Q <sub>gd</sub>		-	-	66	nC

### SOURCE-DRAIN DIODE RATINGS & CHARACT. T<sub>c</sub> = 25°C (UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Continuous Source Current (Body Diode)	I <sub>S</sub>	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. (See schematic)	-	-	4.0	A
Pulse Source Current (Body Diode) (1)	I <sub>SM</sub>		-	-	16	A
Diode Forward Voltage (2)	V <sub>SD</sub>	I <sub>F</sub> =4.0A V <sub>GS</sub> =0V T <sub>c</sub> =+25°C	-	-	1.8	V
Reverse Recovery Time	t <sub>rr</sub>	T <sub>c</sub> =+25°C I <sub>F</sub> =4.0A di/dt=100A/μS	-	800	-	ns

(1) T<sub>J</sub> = 25°C to 150°C.  
(2) Pulse test: Pulse Width < 300μS, Duty Cycle < 2%.  
(3) Repetitive Rating: Pulse Width limited By Max. junction Temperature.