

N-CHANNEL ENHANCEMENT MOS FET

ABSOLUTE MAXIMUM RATINGS			
PARAMETER	SYMBOL		UNITS
Drain-source Volt.(1)	V _{DSS}	600	V _{dc}
Drain-Gate Voltage (R _{GS} =1.0M Ω) (1)	V _{DGR}	600	V _{dc}
Gate-Source Voltage Continuous	V _{GS}	± 20	V _{dc}
Drain Current Continuous (T _c = 25°C)	I _D	17	A _{dc}
Drain Current Pulsed(3)	I _{DM}	68	A
Total Power Dissipation	P _D	300	W
Power Dissipation Derating > 25°C		2.4	W/°C
Operating & Storage Temp.	T _J /T _{sig}	-55 TO +150	°C
Thermal Resistance	R _{thJc}	0.42	°C/W
Max. Lead temperature	TL	300	°C

ELECTRICAL CHARACTERISTICS T _c = 25°C (UNLESS OTHERWISE SPECIFIED)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Drain-source Breakdown Volt.	V _{(BR)DSS}	V _{GS} =0V I _D =250 μ A	600	-	-	V
Gate Threshold Voltage	V _{GS(TH)}	V _D =V _{GS} I _D =250 μ A	2.0	-	4.5	V
Gate Source Leakage	I _{GSS}	V _{GS} = ± 20 V	-	-	100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _D =MAX. RATING V _{GS} =0	-	-	250	μ A
		V _D =0.8 MAX. RATING V _{GS} =0 T _J =125°C	-	-	1000	μ A
Static Drain-Source On-State Resistance(1)	R _{DS(ON)}	V _{GS} =10 V I _D =8.5A	-	-	0.4	Ω
Forward Trans-Conductance (2)	g _{fs}	V _D \geq 50 V I _D =8.5A	9.0	-	-	S(V)
Input Capacitance	C _{ISS}	V _{GS} =0V V _D =25 V f=1.0 MHz	-	4500	-	pF
Output Capacitance	C _{OSS}		-	550	-	pF
Reverse Transfer Capacitance	C _{RSS}		-	160	-	pF
Turn-On Delay	t _{d(on)}	V _{DD} =300V Z _o =50 Ω I _D =8.5A	-	-	100	ns
Rise Time	t _r	(MOSFET switching times are essentially independent of operating temp.)	-	-	110	ns
Turn-Off Delay	t _{d(off)}		-	-	220	ns
Fall Time	t _f		-	-	105	ns
Total Gate Charge (Gate-Source Plus Gate-Drain)	Q _g	V _{GS} =10V, I _D =17A	-	165	-	nC
Gate-Source Charge	Q _{gs}	V _D =0.8 MAX. RATING (Gate charge is essentially independent of the operating temperature)	-	65	-	nC
Gate-Drain ("Miller") Charge	Q _{gd}		-	100	-	nC

SOURCE-DRAIN DIODE RATINGS & CHARACT. T _c = 25°C (UNLESS OTHERWISE SPECIFIED)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Continuous Source Current (Body Diode)	I _S	Modified MOSFET symbol showing the integral reverse P-N junction rectifier (See schematic)	-	-	17	A
Pulse Source Current (Body Diode) (1)	I _{SM}		-	-	68	A
Diode Forward Voltage (2)	V _{SD}	I _F =17A V _{GS} =0V T _c =+25°C	-	-	1.5	V
Reverse Recovery Time	t _{rr}	T _c =+25° C I _F =17A	-	500	-	ns
Reverse Recovery Charge	Q _{rr}	di/dt=100A/ μ S	-	8.0	-	μ C

- (1) T_J = 25°C to 150°C.
 (2) Pulse test: Pulse Width < 300 μ S, Duty Cycle < 2%.
 (3) Repetitive Rating: Pulse Width limited By Max. junction Temperature.

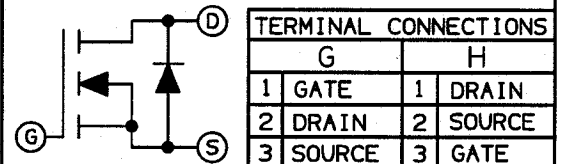
600V, 17A, 0.40 Ω

SDF17N60 GAF

FEATURES

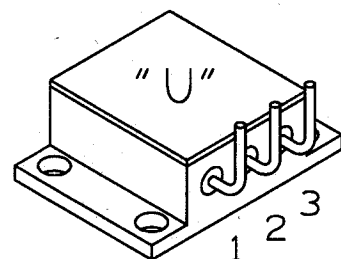
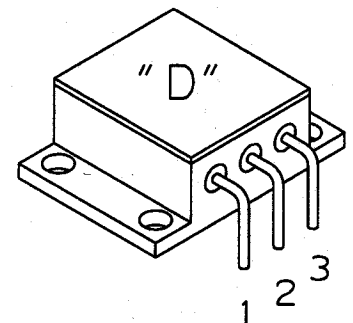
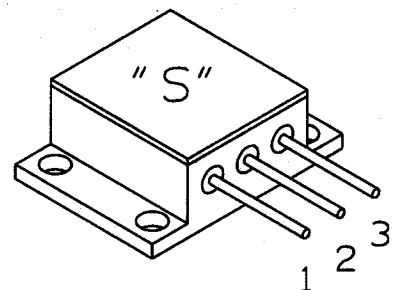
- RUGGED PACKAGE
- HI-REL CONSTRUCTION
- CERAMIC EYELETS
- LEAD BENDING OPTIONS
- COPPER CORED 52 ALLOY PINS
- LOW IR LOSSES
- LOW THERMAL RESISTANCE
- OPTIONAL MIL-S-19500 SCREENING

SCHEMATIC



STANDARD BEND CONFIGURATIONS

GAF



(CUSTOM BEND OPTIONS AVAILABLE)