400V, 100A, 0.05Ω

SDF100NA40 HI
SDF100NA40 JD

FEATURES

- RUGGED PACKAGE
- HI-REL CONSTRUCTION
- CERAMIC EYELETS
- LEAD BENDING OPTIONS
- COPPER CORED 52 ALLOY PINS
- LOW IR LOSSES
- LOW THERMAL RESISTANCE
- OPTIONAL MIL-STD-883 SCREENING

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL		UNITS
DRAIN-SOURCE VOLTAGE	VDSS	400	Vdc
DRAIN-GATE VOLTAGE (R_{GS}=1.0MΩ)	VDGR	400	Vdc
GATE-SOURCE VOLTAGE CONTINUOUS	VGS	±20	Vdc
DRAIN CURRENT CONTINUOUS (Tc = 25°C)	ID	100	Adc
DRAIN CURRENT PULSED	IDM	400	A
TOTAL POWER DISSIPATION	PD	833	W
POWER DISSIPATION DERATING > 25°C		6.67	W/°C
OPERATING & STORAGE TEMP.	TJ/Tsig	-55 TO +150	°C
THERMAL RESISTANCE	RthJc	0.15	°C/W
MAX. LEAD TEMPERATURE	TL	300	°C

ELECTRICAL CHARACTERISTICS PER MOSFET LEG

T_C = 25°C (UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
DRAIN-SOURCE BREAKDOWN VOLTAGE (1 & 2)	V(BR)DSS	VGS=0V ID=250 µA	400	-	-	V
GATE THRESHOLD VOLTAGE	VGS(TH)	VDS=VGS ID=250 µA	2.0	-	4.0	V
GATE SOURCE LEAKAGE	IGSS	VGS=±20 V	-	-	100	nA
ZERO GATE VOLTAGE DRAIN CURRENT	IDSS	VDS=MAX.RATING VGS=0	-	-	250	µA
		VDS=0.8 MAX.RATING VGS=0 TJ=125°C	-	-	1000	µA
STATIC DRAIN-SOURCE ON-STATE RESISTANCE (2)	RDS(ON)	VGS=10 V ID=13A	-	-	0.20	Ω
FORWARD TRANSCONDUCTANCE (2)	gfs	VDS ≥ 50 V IDS=13A	14	-	-	S(℧)
INPUT CAPACITANCE	CISS	VGS=0V VDS=25 V f=1.0 MHz (3)	-	4100	-	pF
OUTPUT CAPACITANCE	COSS		-	480	-	pF
REVERSE TRANSFER CAPACITANCE	CRSS		-	84	-	pF
TURN-ON DELAY	td(on)	VDD=200V RG=4.3Ω ID=25A RD=7.5Ω (MOSFET SWITCHING TIMES ARE ESSENTIALLY INDEPENDENT OF OPERATING TEMP. NOTE 3)	-	-	33	ns
RISE TIME	tr		-	-	140	ns
TURN-OFF DELAY	td(off)		-	-	120	ns
FALL TIME	tf		-	-	99	ns
TOTAL GATE CHARGE (GATE-SOURCE PLUS GATE-DRAIN)	Qg	VGS=10V, ID=25A VDS=0.8 MAX.RATING (GATE CHARGE IS ESSENTIALLY INDEPENDENT OF THE OPERATING TEMPERATURE NOTE 3)	-	-	190	nC
GATE SOURCE CHARGE	Qgs		-	-	27	nC
GATE-DRAIN ("MILLER") CHARGE	Qgd		-	-	93	nC

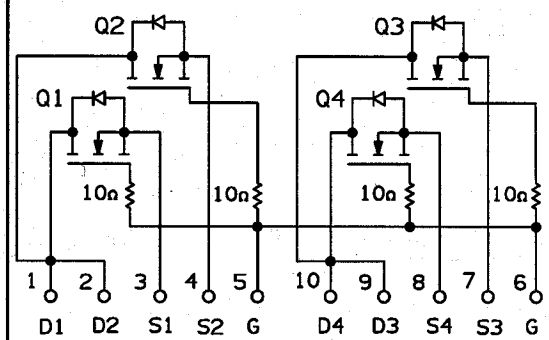
TOTAL MODULE RATINGS AND CHARACTERISTICS

T_C = 25°C (UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNITS
PIN-CASE ISOLATION	PCI	VCASE-PINS ALL PINS SHORTED TO CASE	10	-	mΩ
STATIC DRAIN-SOURCE ON-STATE VOLTAGE	VDS(ON)	VGS ≥ 10V ID = 100A	-	5.0	V
STATIC DRAIN-SOURCE ON-STATE RESISTANCE	RDS(ON)	VGS = 10V ID = 50A	-	0.05	OHM
ZERO GATE VOLTAGE DRAIN CURRENT	IDSS	VGS = 0V VDS = 400V	-	1.0	mA

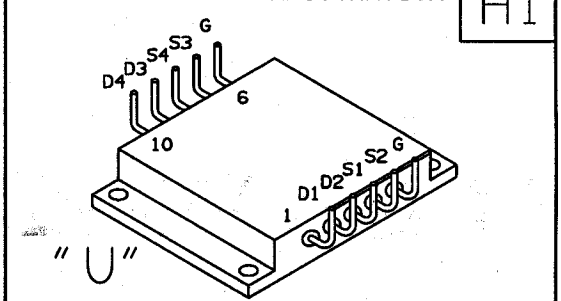
(1) TJ = 25°C TO 150°C.
(2) PULSE TEST: PULSE WIDTH <300µS, DUTY CYCLE <2%.
(3) TEST ARE PERFORMED AT ELEMENT EVALUATION. TEST CONDITIONS AND LIMITS APPLY TO EACH MOSFET SEPARATELY.

SCHEMATIC



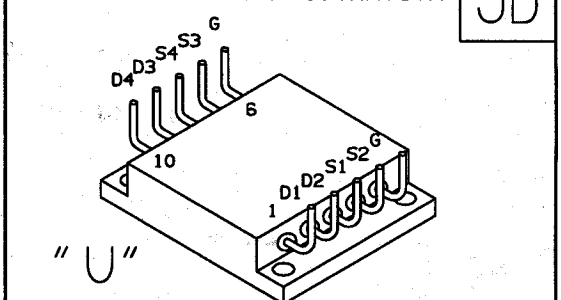
(CUSTOM SCHEMATIC OPTIONS AVAILABLE)

STANDARD BEND CONFIGURATION **HI**



(CUSTOM BEND OPTIONS AVAILABLE)

STANDARD BEND CONFIGURATION **JD**



(CUSTOM BEND OPTIONS AVAILABLE)